CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed over the substrate; and

a control electrode formed over the insulating layer, the control electrode comprising:

a first conductive layer formed over the insulating layer having a first lateral dimension;

a second conductive layer formed over the first conductive layer having the second lateral dimension; and

a non-insulating layer formed over the second conductive layer having a third lateral dimension, the third lateral dimension being greater than the first lateral dimension and greater than the second lateral dimension.

2. The semiconductor device of claim 1, further comprising source/drain regions formed in the substrate.

3. The semiconductor device of claim 1, further comprising a halo implant in the substrate.

4. The semiconductor device of claim 1, wherein the non-insulating layer comprises polysilicon.

5. The semiconductor device of claim 1, wherein the first conductive layer comprises one of tantalum carbide, tantalum nitride, nickel silicide, tantalum silicide, cobalt silicide, or tungsten.

6. The semiconductor device of claim 1, wherein the first conductive layer comprises one of titanium nitride, rhenium, platinum, ruthenium oxide, rhodium silicide, palladium silicide, or tungsten carbon nitride.

7. The semiconductor device of claim 1, wherein the first conductive layer is between 1 and 40 nanometers thick.

8. The semiconductor device of claim 1, wherein the second conductive layer comprises silicon germanium.

9. The semiconductor device claim 1, wherein the second conductive layer comprises one of doped silicon germanium, doped silicon, doped silicon carbide, silicide, metal carbide or metal nitride.

10. The semiconductor device of claim 1, wherein the insulating layer comprises one of hafnium oxide, aluminum nitride, aluminum oxide, tantalum pentoxide, barium titanium oxide, lanthanum aluminate, or zirconium oxide.

11. The semiconductor device of claim 1, wherein the third lateral dimension is made greater than the first lateral dimension and the second lateral dimension by selectively removing portions of the first and second conductive layers to create notches on opposite sides of the control electrode.

12. The semiconductor device of claim 11, wherein the notches are created by selectively etching the second conductive layer and selectively etching the first conductive layer.

13. The semiconductor device of claim 11, wherein the portions of the first conductive layer are removed by oxidation of the portions of the first conductive layer.

14. The semiconductor device of claim 11, wherein a second insulating layer is formed in the notches and on the opposite sides of the control electrode.

15. The semiconductor device of claim 13, further comprising sidewall spacers formed on the second insulating layer on the opposite sides and in the notches of the control electrode.

16. A method for forming a semiconductor device comprising:

providing a substrate having a surface;

forming an insulating layer over the surface of the substrate;

forming a first patterned conductive layer over the insulating layer;

forming a second patterned conductive layer over the first patterned conductive layer;

forming a patterned non-insulating layer over the second patterned conductive layer; and

selectively removing portions of the first and second patterned conductive layers to form a notched control electrode for the semiconductor device.

17. The method of claim 16, further comprising implanting source/drain regions in the substrate.

18. The method of claim 16, further comprising forming a halo implant in the substrate.

19. The method of claim 16, wherein forming the patterned non-insulating layer comprises forming the patterned non-insulating layer of polysilicon.

20. The method of claim 16, wherein the first patterned conductive layer comprises one of tantalum carbide, tantalum nitride, nickel silicide, tantalum silicide, cobalt silicide, or tungsten.

21. The method of claim 16, wherein the first patterned conductive layer comprises one of titanium nitride, rhenium, platinum, ruthenium oxide, rhodium silicide, palladium silicide, or tungsten carbon nitride.

22. The method of claim 16, wherein the first patterned conductive layer is formed to a thickness of between 1 and 40 nanometers.

23. The method of claim 16, wherein the second patterned conductive layer comprises silicon germanium.

24. The method of claim 16, wherein the second patterned conductive layer comprises one of doped silicon germanium, doped silicon, doped silicon carbide, silicide, metal carbide or metal nitride.

25. The method of claim 16, wherein the insulating layer comprises one of hafnium oxide, aluminum nitride, aluminum oxide, tantalum pentoxide, barium titanium oxide, lanthanum aluminate or zirconium oxide, or combinations thereof.

26. The method of claim 16, wherein selectively removing portions of the first and second patterned conductive layers further comprises:

selectively etching a predetermined portion of an exposed lateral edge of the second patterned conductive layer; and

oxidizing an exposed portion of the first patterned conductive layer.

27. The method of claim 16, wherein selectively removing portions of the first and second patterned conductive layers further comprises:

selectively etching a predetermined portion of an exposed lateral edge of the second patterned conductive layer; and

selectively etching an exposed portion of the first patterned conductive layer of the using a soft etch semiconductor manufacturing process.

28. The method of claim 16, further comprising forming a second insulating layer in the notches and on the opposite sides of the notched control electrode.

29. The method of claim 16, further comprising forming sidewall spacers on the second insulating layer on the opposite sides and in the notches of the notched control electrode.